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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,076	11/13/2001	Craig Nemecek	CYPR-CD01210M	4880

7590 08/10/2006

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,076	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action dated 21 November 2005. Applicants' response has amended claims 2 and 16. Claims 1-20 have been submitted for reconsideration.

Claims 1-20 have been rejected.

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 May 2006 has been entered.

Drawings

2. The drawings are objected to because the hand drawn features in FIGS. 2 and 3 are illegible. See 37 CFR 1.83(p). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be

necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Applicants' response states:

> [N]ewly amended Figures 2 and 3 in compliance with 37 CFR 1.121(d) and 37 CFR 1.83(p) are submitted and withdrawal of the objection is earnestly requested.

These newly amended drawings were not found with the papers received by the Office. The Examiner respectfully requests that they be resubmitted.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 7, 8, and 19 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claims 7, 8, and 19 depend from system claims 1 and 15. In either case, these systems are defined in terms of tangible components and are therefore interpreted as falling into the "machine" statutory category of invention. Claims 7, 8, and 19, however, recite a step of how that machine is to be used (*"wherein a user compares* [memory] *when execution of the microcontroller code is halted"* and *"a user compares a state ... when execution of the*

microcontroller code is halted"). These steps do not further define the structural aspects or functional behavior of the system, but rather describe how a person (*"user"*) might employ the invention.

According to MPEP 2173.05(p), claims 7, 8, and 19 are directed to neither a "process" nor a "machine" but rather embrace or overlap two different statutory classes of invention set forth in 35 U.S.C. § 101. Claims 7, 8, and 19 are therefore nonstatutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7, 8, and 19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For the reasons set forth above and according to MPEP 2173.05(p), claims 7, 8, and 19 are directed to neither a "process" nor a "machine" and are therefore indefinite under 35 U.S.C. § 112.

Claim Rejections - 35 USC § 102

In response to the previous rejection of claims 1-2, 5-11, 13-16, and 18-20 under 35 U.S.C. § 102 as being anticipated by US Patent No. 5,371,878 to Coker, Applicants argue that:

> The Applicant does not understand Coker to teach or suggest that the lock step operation is by executing the same instructions using the same clocking signals, as claimed.

Applicants' argument has been fully considered and has been found persuasive. The previous rejection of claims 1-2, 5-11, 13-16, and 18-20 under 35 U.S.C. § 102 has been withdrawn.

Claim Rejections - 35 USC § 103

In response to the previous rejection of claims 3, 12, and 17 as being obvious over Coker in view of US Patent No. 6,173,419 to Barnett, Applicants argue that these claims depend from 1, 9, and 15, respectively, and overcome these references for the same reasons as the independent claims. Applicants' argument has been fully considered and has been found persuasive. The previous rejection of claims 3, 12, and 17 under 35 U.S.C. § 103 has been withdrawn.

In response to the previous rejection of claim 4 as being obvious over Coker in view of "State of the Art" by Stan Augarten, Applicants argue that this claim depends from 1 and overcomes these references for the same reasons as the independent claim. Applicants' argument has been fully considered and has been found persuasive. The previous rejection of claim 4 under 35 U.S.C. § 103 has been withdrawn.

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

5. Claims 1-2, 5-11, 13-16, and 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,357,626 to Johnson et al. (Johnson) in view of US Patent No. 6,366,878 to Grunert and further in view of US Patent No. 4,176,258 to Jackson.

Regarding claims 1, 9, 11, and 15, Johnson teaches a system for debugging code [*"The present invention is generally directed to an arrangement for verifying, with an in circuit emulator, the instructions to be executed by a processor of a processing system."* (column 1, lines 10-13)] comprising:

A processor installed on a test circuit, wherein the processor includes a first memory and a first CPU [FIG. 1, references 12 and 13; *"As thus far described, the microprocessors 12 and 14 are configured for executing instructions stored externally in the external memory 16."* (column 5, lines 12-14); *"However, as will be noted in FIG. 1, each of the processors 12 and 14 includes an internal instruction cache 13 and 15 respectively."* (column 5, lines 44-49)];

An ICE (in circuit emulator) including a second memory and a second CPU coupled to a computer system [FIG. 1, references 14, 15, and 18; *"As will be seen hereinafter, the system 10 is configured to permit the in circuit emulator 18 to verify the execution by the processors 12 and 14 of the execution instructions to be executed by the processors."* (column 3, lines 53-56)];

Wherein the ICE emulates the processor [*"To enable the second processor 14 to duplicate the executions of the first processor 12, the second processor 14 includes a multiple-bit instruction/data input 36 which is coupled to the external instruction/data bus 34."* (column 4, lines 31-34)];

The processor and the ICE run the processor code in lock step by executing the same instructions using the same clocking signals [*"To control system timing, the first processor 12 includes a clock input 40 and the second processor 14 includes a clock input 42. The clock inputs 40 and 42 are coupled together by an INCLOCK line 44 which is adapted to be coupled to an external clock source (not shown)."* (column 4, lines 35-40)]; and

An interface for coupling the test circuit and the ICE [FIG. 1, reference 34, etc.; *"To enable the second processor 14 to duplicate the executions of the first processor 12, the second processor 14 includes a multiple-bit instruction/data input 36 which is coupled to the external*

instruction/data bus 34." (column 4, lines 31-34)], that interface does not prevent transmission between the test circuit and the computer system.

Johnson does not expressly teach that the processors are microcontrollers.

Grunert teaches the use of microcontrollers (abstract). In particular, Grunert teaches two microcontrollers operating in lock step, wherein the second microcontroller emulates the first microcontroller [*"The overall circuit arrangement 1, shown in FIG. 1, for in-circuit emulation includes two microcontrollers 2, 3... The microcontroller 2 is operated as master, the microcontroller 3 as slave"* (column 4, lines 26-39); *"The emulation operation is controlled by means of a service computer connected to the circuit arrangement 1."* (column 5, lines 10-25); *"In accordance with another feature of the invention, a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)].

Johnson and Grunert are analogous art because they are from the same field of endeavor of in-circuit emulation.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Johnson system by replacing the processors 12 and 14 with microcontrollers as taught by Grunert.

The motivation for doing so would have been to verify the operating program of a production microcontroller. Grunert teaches how to easily access this operating program [*"In particular, there is a need to provide a possibility of access to the operating program of the*

microcontroller, which in normal operation is stored in an ROM memory which is not directly accessible from outside." (column 1, lines 9-22)].

Therefore, it would have been obvious to combine Grunert with Johnson to obtain the invention.

Johnson in view of Grunert does not expressly teach comparing contents of a first memory against contents of the second memory to verify the lock step operation.

Jackson teaches comparing contents of a first memory against a contents of a second memory to verify lock step operation [*"The inputs of the chips are externally wired in parallel, and since the chips receive the same input data, they should each generate the same output at any instant of time."* (column 1, lines 46-66); *"The invention has the advantage that when operating properly, both chips should be in exactly the same state throughout all time and therefore the outputs should agree."* (column 1, line 67 – column 2, line 2); and more generally, *"Redundant checking systems are well known in prior art. For example, in the past, two identical logic circuits have been wired in parallel, the same input information being supplied to each, with the output of each circuit being compared in a comparison checking circuit for equality. For example, two identical computers have been operated side-by-side with the same problem being supplied to each. A comparison of the results from each computer at some point in the computation indicates whether one of the computers has malfunctioned."* (column 1, lines 11-21)].

Jackson and Johnson in view of Grunert are analogous art because both are directed to verifying the operation of computer hardware or software.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to compare the outputs of the microcontroller processors (*i.e. register contents or stored memory contents*) to verify lock step operation.

The motivation for doing so would have been to determine whether one of the microcontrollers had malfunctioned, as expressly taught by Jackson and described by Jackson as well known in the art (Jackson, column 1, lines 11-21).

Therefore, it would have been obvious to combine Jackson with Johnson in view of Grunert to obtain the invention as specified in claim 1.

Regarding claims 2, and 16, Grunert teaches that the microcontroller is installed on a pod [*"It is expedient for the microcontrollers 2, 3 to be arranged right next to one another on the printed circuit board, in order to be able to achieve as high an operating frequency as possible. A clock system 5 ensures good synchronization between master 2 and slave 3."* (column 5, lines 5-9)].

Regarding claims 5 and 18, Grunert teaches that the microcontrollers have a plurality of registers [*"The corresponding ports P5', P6', are therefore free in the slave 3, with the result that they can be used for inputting and outputting further internal signals and states, for example*

internal buses, control signals, ***register contents****, etc. or for controlling the program execution."* (column 5, lines 10-25)].

Regarding claim 6, Johnson teaches that the first CPU and second CPU each have a program counter which are maintained in lock step [*"To that end, and as will be more fully described hereinafter, the first processor 12 and second processor 14 are coupled together in a master/slave configuration to permit the second processor 14, which is the slave processor, to duplicate the instructions performed by the first processor 12, which is the master processor."* (column 3, lines 57-62)].

Regarding claims 7, 8, 14, and 19, Jackson teaches comparing the outputs of the microcontroller processors (*i.e. register contents or stored memory contents*) to verify lock step operation. There appears to be no suggestion in any of the cited references that a person would be unable to do so when the execution of the code is halted.

Regarding claim 10, Johnson teaches locating an error within the test code by tracing the execution history using a trace buffer [*"As thus far described, the system 10 is capable of providing the in circuit emulator 18 with sufficient information to track the executions of the processors 12 and 14 of external instructions stored in the external memory 16."* (column 5, lines 40-44) describes "tracing" the execution history; *"This, when combined with the information of when the pipeline is advanced, stalled, branching, or taking a trap, can give the in circuit emulator the instruction trace information it needs."* (column 6, lines 4-8)].

Regarding claims 13 and 20, Grunert teaches that the microcontroller is a production microcontroller [*"When the standard commercially manufactured microcontroller is present, in-circuit emulation is also already possible. It is advantageous that all design changes carried out in the standard commercially manufactured product (for example time response of connecting ports and switching edges, live currents, etc.) are also directly available in the emulator."* (column 1, lines 59-65)].

6. Claims 3, 12, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Grunert and further in view of Jackson, as applied to claims 1, 9, and 15 above, and further in view of US Patent No. 6,173,419 to Barnett.

Regarding claims 3, 12 and 17, none of Johnson, Grunert or Jackson expressly teaches that the microcontroller is copied in an FPGA.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55).

Barnett and Johnson in view of Grunert and further in view of Jackson are analogous art because all are directed to computer hardware.

Therefore it would have been obvious to a person of ordinary skill at the time of Applicants' invention to copy a microcontroller in an FPGA of the emulator.

The motivation for doing so would have been to produce a reconfigurable emulator [*"The emulator is programmed into a field programmable gate array (FPGA) which will work in real time, does not need to be fabricated as an expensive ASIC, and is programmable to other configurations."* (column 5, lines 31-36)].

Therefore it would have been obvious to combine Barnett with Johnson in view of Grunert and further in view of Jackson to obtain the invention as specified in claims 3, 12, and 17.

7. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Grunert and further in view of Jackson, further in view of "State of the Art" by Stan Augarten, published 1983 (Augarten).

None of Johnson, Grunert, or Jackson expressly teaches that the first and second memories are SRAM.

Augarten discloses that SRAM has been known in the art since 1970. Augarten expressly teaches the advantages of SRAM [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing" ... "this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)]

Augarten and Johnson in view of Grunert and further in view of Jackson are analogous art because all are directed computer hardware.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use the well-known technology of SRAM in the microcontrollers.

The motivation would have been avoiding the need to periodically refresh the charges and to store more data in a smaller space [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing"* ... *"this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)].

Therefore, it would have been obvious to combine Augarten with Johnson in view of Grunert and further in view of Jackson to obtain the invention as specified in claim 4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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8/7/06

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